WORKSHOP PROPOSAL

"TANNER TOOL (DIGITAL VLSI)"

Submitted by: -

E2MATRIX

(An ISO 9001:2008 Certified Company)

"Join hands for long relations because trust matter"

Tanner Tools is a software suite for the design, layout and verification of analog, mixed-signal, RF and MEMS ICs. It is an efficient path from design capture through verification. T-Spice Pro helps integrate your design flow from schematic capture through simulation and waveform viewing. L-Edit Pro is a comprehensive physical layout and verification system that accelerates design cycles. It is ideal for applications including Power Management, Life Sciences / Biomedical, Displays, Image Sensors, Automotive, Aerospace, RF, Photovoltaic, Consumer Electronics and MEMS.

Tanner tool is a Spice Computer Analysis Programmed for Analogue Integrated Circuits. Tanner tool consists of the following Engine Machines: S-EDIT (Schematic Edit), T-EDIT (Simulation Edit), W-EDIT (Waveforms Edit), L-EDIT (Layout Edit)

Using these engine tools, spice program provides facility to the use to design & simulate new ideas in Analogue Integrated Circuits before going to the time consuming & costly process of chip fabrication.

The main purpose of this "Hands-on Training on Tanner" is to create awareness and enrich knowledge for research scholars, faculty and students in the area of VLSI using Tanner.

1-DAY WORKSHOP

1. Introduction to VLSI
2. Market Trends
3. Applications of VLSI design
4. Back End Design Overview
5. Design Capabilities
6. Power Management Techniques Needs & Advantages
7. Low Power Design Methodologies
8. Design Tools Available for Low Power
9. Discussion of Low Power Techniques
10. Power Gating (Leakage Reduction)
11. Sleep Methods (Static Power Reduction)
12. Adiabatic Technique (Heat Power Reduction)
13. Clock Gating Methods
14. Low Power Design Technologies & Tools
15. Tanner EDA Workflow
16. S-EDIT, W-EDIT, TSPICE

TIME DURATION: 4 hours

COST: 200/- PER STUDENT

2-DAYS WORKSHOP

Module 1

1. Introduction to VLSI
2. Market Trends
3. Applications of VLSI design
4. Back End Design Overview
5. Design Capabilities
6. Power Management Techniques Needs & Advantages
7. Low Power Design Methodologies
8. Design Tools Available for Low Power
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10. Power Gating (Leakage Reduction)
11. Sleep Methods (Static Power Reduction)
12. Adiabatic Technique (Heat Power Reduction)
13. Clock Gating Methods
14. Low Power Design Technologies & Tools
15. Tanner EDA Workflow
16. S-EDIT, W-EDIT, TSPICE

Module 2

1. Tanner EDA Lab
2. CMOS Inverter Design
3. Power Gating Technique for CMOS Full Adder
4. Power Calculation of a Circuit using TSPICE
5. Different methods of Power Calculation
6. Power Calculation of an Logical Gates
7. Design of Clock Gating Method

8. Methods to design a Clock Gating Circuit
9. Design and Analysis of Data Driven Clock Gating
10. Design of Embedded Logic in Flip Flops
11. Advantages of Embedded Logic
12. How to merge a logical circuit into a Flip Flop circuit
13. Design and Analysis of an Embedded Logic Gate

TIME DURATION: 4 hours

COST: 300/- PER STUDENT

3-DAYS WORKSHOP

Module 1

1. Introduction to VLSI
2. Market Trends
3. Applications of VLSI design
4. Back End Design Overview
5. Design Capabilities
6. Power Management Techniques Needs & Advantages
7. Low Power Design Methodologies
8. Design Tools Available for Low Power
9. Discussion of Low Power Techniques
10. Power Gating (Leakage Reduction)
11. Sleep Methods (Static Power Reduction)
12. Adiabatic Technique (Heat Power Reduction)
13. Clock Gating Methods
14. Low Power Design Technologies & Tools
15. Tanner EDA Workflow
16. S-EDIT, W-EDIT, TSPICE

Module 2

1. Tanner EDA Lab
2. CMOS Inverter Design
3. Power Gating Technique for CMOS Full Adder
4. Power Calculation of a Circuit using TSPICE
5. Different methods of Power Calculation
6. Power Calculation of an Logical Gates

Module 3

1. Design of Clock Gating Method
2. Methods to design a Clock Gating Circuit
3. Design and Analysis of Data Driven Clock Gating
4. Design of Embedded Logic in Flip Flops
5. Advantages of Embedded Logic
6. How to merge a logical circuit into a Flip Flop circuit
7. Design and Analysis of an Embedded Logic Gate
8. Design of Data Driven Clock Gating
9. Design of D Flip Flop with Embedded Logic Module

TIME DURATION: 4 hours /day

COST: 500/- PER STUDENT